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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,687	10/27/2003	Kazuto Usuda	030712-15	2065

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EXAMINER	
ALIA, CURTIS A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/692,687	**Applicant(s)** USUDA ET AL.	
	Examiner Curtis A. Alia	**Art Unit** 2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7,8 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,8 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7 April 2009 has been entered.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Response to Amendment

Applicant's amendment filed on 7 April 2009 has been entered. Claims 6 and 9 have been cancelled. Claims 1, 2, 4, 5, 7, 8 and 10-15 are still pending in this application, with claims 1 and 10 being independent.

Response to Arguments

2. Applicant's arguments with respect to claims 1-2 and 4-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 1, 2, 4, 5, 7, 8 and 10-15 are objected to because of the following informalities: The first instance of acronyms FIFO and VCO in each claim set should be written out in parentheses. For example, on line 1 of claim 1, "FIFO" should read --- First In First Out (FIFO) buffer ---. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. On line 5, the phrase "delete a specified packet when from an input side" seems to contain a typo.

Claim Rejections - 35 USC § 103

5. Claims 1, 2, 4, 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc (newly cited US 2004/0057445, priority date September 20, 2002) in view of Kramer et al. (newly cited US 6,658,027).

Regarding claim 1, LeBlanc discloses a method of controlling a jitter buffer using a FIFO, comprising the steps of: setting a packet delete area, a packet add area, and a clock control area inside the FIFO (see paragraph 33, within the jitter buffer there is a section receiving packets with thresholds (delete area), a middle section (clock control area), and a section sending

packets to the receiver with thresholds (add area)), raising a clock frequency when the stored packet quantity of the FIFO reaches an upper limit of the clock control area (see paragraph 33, if the fill level of the jitter buffer reaches an upper threshold, then the retrieval rate (clock frequency) is increased so as to keep the buffer from overflowing), lowering the clock frequency when the stored packet quantity of the FIFO reaches a lower limit of the clock control area (see paragraph 33, if the fill level of the jitter buffer reaches a lower threshold, then the retrieval rate (clock frequency) is decreased so as to keep the buffer from reaching an underflow condition).

LeBlanc does not explicitly teach controlling a stored packet quantity of the FIFO to delete a specified packet when from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area, and to delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area or controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to add the packets when the stored packet quantity falls below a lower limit of the packet add area or setting the clock control area between the packet add area and the packet delete area.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches controlling a stored packet quantity of the FIFO to delete a specified packet when from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area, and to delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area (see column 5, lines 5+, when the fill level of the jitter buffer reaches a certain threshold close to the end of the buffer (delete area), it is determined that frames may be deleted from that level so as to keep the level from rising past

that threshold value) and controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to add the packets when the stored packet quantity falls below a lower limit of the packet add area (see column 5, lines 5+, when the fill level of the jitter buffer reaches a certain minimum threshold close to the front of the buffer (add area), it is determined that (silence) frames may be added to that level so as to keep the level from dropping to zero) and setting the clock control area between the packet add area and the packet delete area (see paragraph 33 of LeBlanc and column 5 of Kramer, the add and delete areas are located at the edges of the buffer, and the clock is controlled throughout the buffer with multiple threshold levels, some being in the middle of the buffer).

In view of the above, having the method of LeBlanc, then given the well-established teaching of Kramer, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of LeBlanc as taught by Kramer, since Kramer stated that rate mismatches between transmitter and receiver can be more efficiently overcome.

Regarding claim 2, LeBlanc teaches that there are upper limits and lower limits of thresholds in the jitter buffer (see paragraph 33), but does not explicitly teach that the lower limit of the packet add area is equal to the upper limit thereof.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches that the lower limit of the packet add area is equal to the upper limit thereof (see column 5, lines 5+, the add area concentrates on one threshold,

which, when the fill level drops below, invokes the adding of frames into the buffer, so the lower limit and the upper limit are one limit).

In view of the above, having the method of LeBlanc, then given the well-established teaching of Kramer, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of LeBlanc as taught by Kramer, since Kramer stated that rate mismatches between transmitter and receiver can be more efficiently overcome.

Regarding claim 4, LeBlanc discloses that the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control area to the upper limit thereof (see paragraph 33, multiple thresholds are set and the clock maybe linearly increased from one threshold to another, as well as decreased from one threshold to another).

Regarding claim 5, LeBlanc discloses that the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control area to the upper limit thereof (see paragraph 33, multiple thresholds are set and the clock maybe linearly increased from one threshold to another, as well as decreased from one threshold to another).

Regarding claim 7, LeBlanc discloses that the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the

upper limit thereof (see paragraph 33, multiple thresholds are set and the clock may be increased from one threshold to another at a faster rate than the previous threshold, as well as decreased from one threshold to another, where each successively more severe threshold is met, a higher clock rate increase is introduced to compensate).

Regarding claim 8, LeBlanc discloses that the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof (see paragraph 33, multiple thresholds are set and the clock may be increased from one threshold to another at a faster rate than the previous threshold, as well as decreased from one threshold to another, where each successively more severe threshold is met, a higher clock rate increase is introduced to compensate).

6. Claims 10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc in view of Kramer and Gladden et al. (newly cited US 6,738,916).

Regarding claim 10, LeBlanc discloses a device of controlling a jitter buffer, comprising: a FIFO, having an input side and an output side, that configures the jitter buffer, a packet deletion circuit provided on the input side of the FIFO, and a packet addition circuit provided on the output side of the FIFO (see paragraph 33, within the jitter buffer there is a section receiving packets with thresholds (delete area), a middle section (clock control area), and a section sending packets to the receiver with thresholds (add area)), a jitter buffer control circuit that includes a

buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO (see paragraph 33, the fill level of the buffer is monitored), and a buffer control circuit for controlling the operations of the FIFO and peripheral circuits thereof (see figure 3, jitter buffer processor), and

LeBlanc does not explicitly teach that the buffer control circuit controls the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area, and the buffer control circuit controls to add the packets when the stored packet quantity falls below an upper limit of a packet add area.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches that the buffer control circuit controls the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area (see column 5, lines 5+, when the fill level of the jitter buffer reaches a certain threshold close to the end of the buffer (delete area), it is determined that frames may be deleted from that level so as to keep the level from rising past that threshold value), and the buffer control circuit controls to add the packets when the stored packet quantity falls below an upper limit of a packet add area (see column 5, lines 5+, when the fill level of the jitter buffer reaches a certain minimum threshold close to the front of the buffer (add area), it is determined that (silence) frames may be added to that level so as to keep the level from dropping to zero).

LeBlanc and Kramer do not explicitly teach a VCO that supplies to vary a reproduced clock frequency or a decoder that accepts the packets outputted from the packet addition circuit, and decodes frames of the packets based on the clock frequency supplied from the VCO.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Gladden. In particular, Gladden teaches a VCO that supplies to vary a reproduced clock frequency and a decoder that accepts the packets outputted from the packet addition circuit, and decodes frames of the packets based on the clock frequency supplied from the VCO (see column 11, lines 7+, VCO is connected to the jitter buffer in that it supplies voltage controlled clock that has a variable frequency to offset the jitter, the VCO outputs the clock to which the packets are transmitted).

In view of the above, having the system of LeBlanc and Kramer, then given the well-established teaching of Gladden, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the system of LeBlanc and Kramer as taught by Gladden, since Gladden stated that synchronization can be implemented for multiple channel environments.

Regarding claim 12, LeBlanc does not explicitly teach that the jitter buffer control circuit is in direct communication with the packet deletion circuit and the packet addition circuit.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches that the jitter buffer control circuit is in direct communication with the packet deletion circuit and the packet addition circuit (see column 5, lines 5+, the jitter buffer manager (buffer control circuit) makes the determination as to whether to add or delete frames, therefore the jitter buffer manager must be directly signaling to add and/or delete circuits to add/delete frames to/from the buffer).

In view of the above, having the method of LeBlanc, then given the well-established teaching of Kramer, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of LeBlanc as taught by Kramer, since Kramer stated that rate mismatches between transmitter and receiver can be more efficiently overcome.

Regarding claim 13, LeBlanc does not explicitly teach that the packet deletion circuit and the packet addition circuit are in direct communication with the buffer control circuit of the jitter buffer control circuit.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches that the packet deletion circuit and the packet addition circuit are in direct communication with the buffer control circuit of the jitter buffer control circuit (see column 5, lines 5+, the jitter buffer manager (buffer control circuit) makes the determination as to whether to add or delete frames, therefore the jitter buffer manager must be directly signaling to add and/or delete circuits to add/delete frames to/from the buffer).

In view of the above, having the method of LeBlanc, then given the well-established teaching of Kramer, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of LeBlanc as taught by Kramer, since Kramer stated that rate mismatches between transmitter and receiver can be more efficiently overcome.

Regarding claim 14, LeBlanc does not explicitly teach that the jitter buffer control circuit is in direct communication with the jitter buffer.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches the jitter buffer control circuit is in direct communication with the jitter buffer (see figure 1, jitter buffer 120 is in direct communication with jitter buffer manager).

In view of the above, having the method of LeBlanc, then given the well-established teaching of Kramer, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of LeBlanc as taught by Kramer, since Kramer stated that rate mismatches between transmitter and receiver can be more efficiently overcome.

Regarding claim 15, LeBlanc does not explicitly teach that the jitter buffer is in direct communication with a buffer monitoring portion of the jitter buffer control circuit.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Kramer. In particular, Kramer teaches that the jitter buffer is in direct communication with a buffer monitoring portion of the jitter buffer control circuit (see figure 2, jitter buffer manager is in direct communication with the buffer monitoring portion (which includes the water marks/thresholds)).

In view of the above, having the method of LeBlanc, then given the well-established teaching of Kramer, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of LeBlanc as taught by Kramer, since Kramer stated that rate mismatches between transmitter and receiver can be more efficiently overcome.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over LeBlanc in view of Kramer and Gladden as applied to claim 10 above, and further in view of Otlean (previously cited US 6,044,113).

Regarding claim 11, LeBlanc, Kramer and Gladden do not explicitly teach that a pulse width modulator is used in replacement for the VCO.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Otlean. In particular, Otlean teaches that a pulse width modulator is used in replacement for the VCO (see abstract, pulse width modulator produces a variable clock signal that is proportional to a voltage input).

In view of the above, having the system of LeBlanc, Kramer and Gladden, then given the well-established teaching of Otlean, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the system of LeBlanc, Kramer and Gladden as taught by Otlean, since Otlean stated that the pulse widths of the highs and lows of the clock signals can be varied independently.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 270-3116. The examiner can normally be reached on Monday through Friday, 9am-6pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2416

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Examiner, Art Unit 2416
6/17/2009

CAA